

REMARKS

Claims 1-53 are pending in the application. Applicant would like to thank the Examiner for indicating that claims 22-53 are allowed and that claims 2, 4, 6-11 and 15-21 are allowable.

Claims 1, 3, 5 and 12-14 are rejected as unpatentable over HIBINO et al. 6,529,251 in view of WANG et al. 6,277,674. This rejection is respectfully traversed.

Claim 1 provides that gate electrodes of TFTs have a first multilevel conductive structure. Claim 1 also provides that scan lines connected to the corresponding gate electrodes have the first multilevel conductive structure. The first multilevel conductor structure includes a TiN film, an Al-based film below the TiN film, and at least one Ti film located at at least one of an upper position and a lower position with respect to the Al-based film.

Figure 3b of HIBINO et al. teaches a three-layer gate electrode structure with a top layer 15 of TiN, a middle layer 14 of Al, and a lower layer 13 of Ti. However, HIBINO et al. fail to teach or suggest scan lines connected to the corresponding gate electrodes and having the first multilevel conductive structure. Moreover, applicants have thoroughly reviewed HIBINO et al. and are unable to discern any teaching regarding a scan line. Accordingly, HIBINO et al. neither disclose nor suggest

the specific scan line connected to the gate electrode and having the first multilevel conductive structure, as recited in claim 1.

WANG et al. is only cited for the teaching of a TiN film having a specific nitrogen concentration. The WANG et al. reference is directed to semiconductor fuses and not to LCD devices and, as such, would not have scan lines. Therefore, WANG et al. do not teach scan lines connected to the corresponding gate electrodes and having the first multilevel conductive structure as recited in claim 1.

The above noted feature is missing from each of the references, is absent from the combination, and thus is not obvious to one having ordinary skill in the art.

Claims 3 and 5 depend from claim 1 and further define the invention and are also believed patentable over the cited prior art.

Claim 12 provides source and drain electrodes having a first multilevel structure and signal lines connected to the corresponding source electrodes having the multilevel structure wherein the multilevel structure includes TiN, Al, and at least one Ti film.

HIBINO et al. only teach a gate electrode having a multilevel structure (of at least three levels). The source electrode of HIBINO et al. is a two-layered structure, not a three-layered structure. In addition, HIBINO et al. do not

disclose or suggest signal lines connected to the corresponding source electrodes having the multilevel structure.

As noted above, WANG et al. is only cited for the specific nitrogen concentration in a TiN layer. WANG et al. neither teach the first multilevel structure nor that source and drain electrodes and signal lines connected to the corresponding source electrodes have the first multilevel structure.

The above-noted features are missing from each of the references, are absent from the combination, and thus are not obvious to one having ordinary skill in the art.

Claims 13 and 14 depend from claim 12 and further define the invention and are also believed patentable over the cited prior art.

In view of the foregoing remarks, it is believed that the present application is in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

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overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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